REMARKS/ARGUMENTS

Restriction of claims to one of groups I-IV has been required under 35 U.S.C. § 121. Group I (claims 1-4, 8, 23-24) is hereby provisionally elected without traverse for continued examination.

The specification stands objected to due to a typographical error noted by the Examiner at page 8, line 14. The specification has been amended accordingly. No new matter has been added.

Claim 1 stands objected to on the basis of a typographical error introduced during preparation of the application, and noted by the Examiner. Claim 1 has been amended to correct the noted typographical error and a further clerical error. No change in the scope of the claim is intended.

Claim 23 has been amended to further clarify the invention.

Claims 1-2, 4 and 8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by United States Patent No. 6,124,741 to Arcus (Arcus).

The claimed invention relates to a charge pump. Page 5, line 13. As shown in figure 4, the charge pump includes a first plurality of serially connected transistors of a first conductivity type, a second plurality of serially connected transistors of a second conductivity type, said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors.

Accordingly, claim 1 recites:

> A charge pump circuit comprising: a first plurality of serially connected transistors of a first conductivity type; a second plurality of serially connected transistors of a second conductivity type; said first plurality of serially connected transistors being serially connected to the second plurality of

serially connected transistors; the interconnection of said first and second plurality of transistors providing an output; a gate of one of said first plurality of transistors being adapted to receive a $\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of another one of said second plurality of transistors being adapted to receive another DC bias signal; and a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a DOWN pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an $\overline{\text{UP}}$ pulse signal." Emphasis added.

In contrast, the Office Action refers to Fig. 9 of the Arcus reference which shows a charge pump "embodiment that can be powered down." Column 10, lines 33-34. "Power down signal PD and its inverse PDB are used in place of ground and the power supply to the gates of various transistors. PD replaces ground to the gates of p-channel transistors 22, 52, 46, and 56, while PDB replaces power to the gates of n-channel transistors 28, 42, 56 and 64." Column 10, lines 34-39. The Office Action has overlooked this definition of terms in the Arcus reference, and thus mistaken Fig. 9 of Arcus for the claimed invention. The application of power-down and inverse power-down signals to respective gates of the present invention would render the claimed invention inoperative. Likewise, application of the UP pulse and $\overline{\text{DOWN}}$ pulse signals of the present invention to respective gates of the Arcus circuit would render the Arcus device inoperative. Accordingly, the Arcus reference does not teach or suggest the claimed invention, and the rejection of claim 1 under 35 U.S.C. § 102(e) over Arcus should be withdrawn.

Claims 2 and 4 depend directly from claim 1 and incorporate every limitation thereof. Accordingly, the rejections of claims 2 and 4 under 35 U.S.C. § 102(e) over Arcus should be withdrawn for the same reasons given above with respect to claim 1.

Claim 8 recites:

> A charge pump circuit comprising: a first plurality of serially connected transistors of a first conductivity type; a second plurality of serially connected transistors of a second conductivity type; said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors; the interconnection of said first and second plurality of transistors providing an output; a gate of one of said first plurality of transistors being adapted to receive a first switching signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive a second switching signal, and a gate of the other of said second plurality of transistors being adapted to receive another DC bias signal; and a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal.

Arcus does not teach or suggest "a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a complementary first switching signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive a complementary second switching signal." Accordingly, the rejection of claim 8 under 35 U.S.C. § 102(e) over Arcus should be withdrawn.

Claims 3 and 23-24 stand rejected under 35 U.S.C. § 103(a) over Arcus.

With respect to claim 3, the Office Action acknowledges that Arcus does not disclose a) a first capacitor circuit for coupling the DOWN pulse signal to the first node, and b) a second capacitor circuit for coupling the UP pulse signal to the second node. The

Office Action alleges, without citing a reference document, that these limitations of claim 3 would have been obvious to one of ordinary skill in the art. Applicant traverse this allegation as lacking proper basis, and further notes that claim 3 depends directly from claim 1. Claim 1 has been shown to contain additional limitations not taught or suggested in the Arcus reference, as discussed above with respect to the rejection of claim 1 under 35 U.S.C. § 102(e). Accordingly, for at least the reasons given above with respect to claim 1, the rejection of claim 3 under 35 U.S.C. § 103(a) over Arcus should be withdrawn.

With respect to claim 23, the Office Action acknowledges that Arcus does not disclose "the steps of a) capacitively coupling a complementary signal of the first applied switching signal to a connection between the first switching transistor and an associated bias transistor; and b) capacitively coupling a complementary signal of the second applied switching signal to a connection between the second switching transistor and an associated bias transistor." The Office Action alleges, without citing a reference document, that these limitations of claim 23 would have been obvious to one of ordinary skill in the art. Applicant traverses this allegation as lacking proper basis and further notes that Arcus also does not teach or suggest the additional limitations of "switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal; switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal; biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors; coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor to maintain a substantially continuously controlled voltage at said output terminal." As discussed above with respect to the rejection of claim 1 under 35 U.S.C. § 102(e), the Arcus circuit of Fig. 9 relates to a Power-down signal, and does not teach or suggest using the PD and PDB signals "to maintain a substantially continuously controlled voltage at said output terminal." Accordingly, Arcus does not teach or suggest the unique combination of

limitations recited in claim 23, and the rejection of claim 23 under 35 U.S.C. § 103(a) over Arcus should be withdrawn.

Claim 24 depends directly from claim 23 and incorporates every limitation thereof. Accordingly, the rejection of claim 24 under 35 U.S.C. § 103(a) over Arcus should be withdrawn for at least the same reasons given above with respect to claim 23.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: April 25, 2002

Respectfully submitted,

By _____ Reg. No. 31,063

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Version With Markings to Show Changes Made

Please rewrite the paragraph on page 8, line 11-page 9, line 2 as follows:

The signal DOWN is applied through capacitor 65 to the common node A of respective switching and D.C. biasing transistors 29 and 43, while the switching signal $\overline{UP}$ is applied through capacitor 69 to the common node [13]B between respective transistors 45 and 31. The provision of the switching signals DOWN and [UP]$\overline{UP}$ to respective nodes A and B provides a fast turn on and turn off of the transistors 29 and 31 without waveform distortion in the resulting output signal. The voltage on the capacitors 65 and 69 settles to a DC point where the voltage across transistors 29 and 31 is minimal, but the net effect is a fast turn on and turn off of transistors 29 and 31 with low capacitively coupled charge injection.

Please rewrite claims 1 and 23 as follows:

1. (Amended) A charge pump circuit comprising:

a first plurality of serially connected transistors of a first conductivity type;

a second plurality of serially connected transistors of a second conductivity type;

said first plurality of serially connected transistors being serially connected to the second plurality of serially connected transistors;

the interconnection of said first and second plurality of transistors providing an output;

a gate of one of said first plurality of transistors being adapted to receive a

$\overline{\text{DOWN}}$ pulse signal, a gate of another one of said first plurality of transistors being adapted to receive a DC bias signal, a gate of one of said second plurality of transistors being adapted to receive an UP pulse signal, and a gate of [the other]another one of said second plurality of transistors being adapted to receive another DC bias signal; and

a first node at the interconnection of transistors of said first plurality of transistors being adapted to receive a [$\overline{\text{DOWN}}$]$\overline{\text{DOWN}}$ pulse signal and a second node at the interconnection of transistors of said second plurality of transistors being adapted to receive an UP pulse signal.

23. (Amended) A method of operating a charge pump comprising:

switching a first switching transistor in response to a first applied switching signal to affect an output at an output terminal;

switching a second switching transistor in response to a second applied switching signal to affect an output at said output terminal;

biasing the switching characteristics of said first and second switching transistors with bias transistors respectively serially connected to said first and second switching transistors;

coupling a complementary signal of said first applied switching signal to a connection between said first switching transistor and an associated bias transistor; and

coupling a complementary signal of said second applied switching signal to a connection between said second switching transistor and an associated bias transistor to maintain a substantially continuously controlled voltage at said output terminal.